C L A I M S

1. A trigger signal generating apparatus comprising:

a frame synchronous circuit which receives a frame signal having a predetermined bit rate and outputs a synchronous signal in synchronism with an input timing of leading data of the frame signal;

a position information output circuit which receives the synchronous signal output by the frame synchronous circuit and outputs position information indicating an input bit position of the frame signal;

a position designator which designates an arbitrary bit position of the frame signal; and

a trigger signal generating circuit which outputs a trigger signal at a timing when the position information output by the position information output circuit is coincident with the arbitrary bit position designated by the position designator.

2. A trigger signal generating apparatus according to claim 1, wherein the frame signal having the predetermined bit rate is a frame signal transmitted through a digital synchronous network.

3. A trigger signal generating apparatus according to claim 2, wherein the frame signal transmitted by the digital synchronous network is that of one of the digital synchronous transmission systems including a synchronous digital hierarchy (SDH),

synchronous optical network (SONET) and optical transport network (OTN).

4. A trigger signal generating apparatus according to claim 3, wherein when the frame signal transmitted by the digital synchronous network is associated with one of the digital synchronous transmission systems including SDH, SONET and OTN, the arbitrary bit position designated by the position designator is a specified part of an overhead of the frame signal of the digital synchronous transmission system.

5. A trigger signal generating apparatus according to claim 4, wherein the specified part of the overhead of the frame signal of the digital synchronous transmission system is not scrambled.

6. A trigger signal generating apparatus according to claim 1, further comprising:

a clock recovery circuit which receives the frame signal having the predetermined bit rate and recovers and outputs a clock from the frame signal.

7. A frame signal waveform observation apparatus comprising:

a trigger signal generating apparatus comprising;

a frame synchronous circuit which receives a frame signal having a predetermined bit rate and outputs a synchronous signal in synchronism with an input timing of leading data of the frame signal,

a position information output circuit which receives the synchronous signal output by the frame synchronous circuit and outputs position information indicating an input bit position of the frame signal,

a position designator which designates an arbitrary bit position of the frame signal, and

a trigger signal generating circuit which outputs a trigger signal at a timing when the position information output by the position information output circuit is coincident with the arbitrary bit position designated by the position designator; and

a sampling oscilloscope which receives the trigger signal output from the trigger signal generating circuit of the trigger signal generating apparatus, sampling the frame signal with a trigger signal input timing as a reference timing and acquiring and displaying waveform information in a neighborhood of the arbitrary bit position designated by the position designator.

8. A frame signal waveform observation apparatus according to claim 7, wherein the sampling oscilloscope has a function of acquiring the waveform information in the neighborhood of designated arbitrary bit position for a plurality of times and averaging them thereby to display averaged waveform information in the neighborhood of the designated arbitrary bit position in such a manner that a phase variation dependent on

a bit pattern of the frame signal can be measured while suppressing the phase variation of random noise type of the frame signal.

9. A frame signal waveform observation apparatus according to claim 7, wherein the frame signal having the predetermined bit rate is transmitted by a digital synchronous network.

10. A frame signal waveform observation apparatus according to claim 9, wherein the frame signal transmitted by the digital synchronous network is that of one of the digital synchronous transmission systems including a synchronous digital hierarchy (SDH), synchronous optical network (SONET) and optical transport network (OTN).

11. A frame signal waveform observation apparatus according to claim 10, wherein when the frame signal transmitted by the digital synchronous network is associated with one of the digital synchronous transmission systems including SDH, SONET and OTN, the bit position designated by the position designator is a specified part of an overhead of the frame signal of the digital synchronous transmission system.

12. A frame signal waveform observation apparatus according to claim 11, wherein the specified part of the overhead of the frame signal of the digital synchronous transmission system is not scrambled.

13. A frame signal waveform observation apparatus

according to claim 7, wherein the trigger signal generating apparatus further comprises a clock recovery circuit which receives the frame signal having the predetermined bit rate and recovers and outputs a clock from the frame signal, and

wherein the sampling oscilloscope of the frame signal waveform observation apparatus acquires and displays waveform information of the clock recovered by the clock recovery circuit in addition to displaying the waveform information in a neighborhood of arbitrary bit position of the frame signal designated by the position designator.

14. A frame signal waveform observation apparatus according to claim 8, wherein the trigger signal generating apparatus further comprises a clock recovery circuit which receives the frame signal having the predetermined bit rate and recovers and outputs a clock from the frame signal, and

wherein the sampling oscilloscope of the frame signal waveform observation apparatus has a function of acquiring waveform information in the neighborhood of designated arbitrary bit position for a plurality of times and averaging them and the function of acquiring the waveform information of the clock recovered by the clock recovery circuit and averaging them, whereby a phase variation of random noise type is suppressed thereby to display the waveform information in the

neighborhood of the designated arbitrary bit position of the frame signal and the averaged waveform information of the clock with the phase variation of random noise type suppressed.

15. A trigger signal generating method comprising:

receiving a frame signal having a predetermined bit rate and outputting a synchronous signal in synchronism with an input timing of leading data of the frame signal;

receiving the synchronous signal and outputting position information indicating an input bit position of the frame signal;

designating an arbitrary bit position of the frame signal; and

outputting a trigger signal at a timing when the position information is coincident with the designated arbitrary bit position.

16. A trigger signal generating method according to claim 15, wherein the frame signal having the predetermined bit rate is transmitted by a digital synchronous network.

17. A trigger signal generating method according to claim 16, wherein the frame signal transmitted by the digital synchronous network is that of one of the digital synchronous transmission systems including a synchronous digital hierarchy (SDH),

synchronous optical network (SONET) and optical transport network (OTN).

18. A trigger signal generating method according to claim 17, wherein when the frame signal transmitted by the digital synchronous network is associated with one of the digital synchronous transmission systems including SDH, SONET and OTN, the arbitrary bit position of the frame signal designated as a trigger signal generating position is a specified part of an overhead of the frame signal of the digital synchronous transmission system.

19. A trigger signal generating method according to claim 18, wherein the specified part of the overhead of the frame signal of the digital synchronous transmission system is not scrambled.

20. A trigger signal generating method according to claim 15, further comprising:

receiving the frame signal having the predeter-mined bit rate and recovering and outputting a clock from the frame signal.

21. A frame signal waveform observation method comprising:

receiving a frame signal having a predetermined bit rate and outputting a synchronous signal in synchronism with an input timing of leading data of the frame signal;

receiving the synchronous signal and outputting

position information indicating an input bit position of the frame signal;

designating an arbitrary bit position of the frame signal;

outputting a trigger signal at a timing when the position information is coincident with the designated arbitrary bit position; and

receiving the trigger signal, sampling the frame signal with a trigger signal input timing as a reference timing and acquiring waveform information of the designated arbitrary bit position of the frame signal.

22. A frame signal waveform observation method according to claim 21, further comprising:

acquiring the waveform information in a neighborhood of the designated arbitrary bit position of the frame signal having the predetermined bit rate repeatedly for a plurality of times;

averaging the waveform information in the neighborhood of the designated arbitrary bit position of the frame signal acquired for the plurality of times; and

suppressing a phase variation of random noise type of the frame signal and displaying the phase variation dependent on a bit pattern of the frame signal in a measurable way, based on the waveform information in the neighborhood of the designated arbitrary bit

position of the frame signal which have been averaged.

23. A frame signal waveform observation method according to claim 21, wherein the frame signal having the predetermined bit rate is transmitted by a digital synchronous network.

24. A frame signal observation method according to claim 23, wherein the frame signal transmitted by the digital synchronous network is that of one of the digital synchronous transmission systems including a synchronous digital hierarchy (SDH), synchronous optical network (SONET) and optical transport network (OTN).

25. A frame signal waveform observation method according to claim 24, wherein when the frame signal transmitted by the digital synchronous network is associated with one of the digital synchronous transmission systems including SDH, SONET and OTN, the bit position designated by the position designator is a specified part of an overhead of the frame signal of the digital synchronous transmission system.

26. A frame signal waveform observation method according to claim 25, wherein the specified part of the overhead of the frame signal of the digital synchronous transmission system is not scrambled.

27. A frame signal waveform observation method according to claim 21, further comprising:

receiving the frame signal having the

predetermined bit rate and recovering and outputting a clock from the frame signal;

acquiring by sampling a waveform information of the clock recovered from the frame signal; and

displaying the waveform information of the clock acquired by sampling.

28. A frame signal waveform observation method according to claim 22, further comprising:

receiving the frame signal having the predetermined bit rate and recovering and outputting a clock from the frame signal;

acquiring, by sampling for a plurality of times, the waveform information of the clock recovered from the frame signal;

averaging the waveform information of the clock acquired by sampling for a plurality of times; and

displaying, as related to each other, averaged waveform information of the clock and the averaged waveform information in the neighborhood of the designated arbitrary bit position of the frame signal in order to make it possible to measure a phase variation dependent on a bit pattern of the frame signal by comparison with the averaged waveform information of the clock while suppressing the phase variation of random noise type of the frame signal.